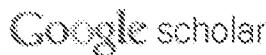


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Current trends in flash memory technology: invited paper

SL Min... - Proceedings of the 2006 Asia and South Pacific ..., 2006 - portal.acm.org
 ... memory drives. Of course, multiple **flash** memory buses can be used for higher bus bandwidth but this approach will require a higher pin count and a bus **interleaving** logic **within** the **flash** memory controller. A preferred approach ...

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Flash memory including a mode register for indicating synchronous or asynchronous mode of operation

DR Mills, BL Dipert, S Sambandan... - US Patent ..., 2000 - Google Patents
 ... Alternately, if a single address is provided to the **flash** chip when it is in the synchronous mode, the subsequent addresses for the burst will be generated **within** the **flash** chip and the data burst will then be provided as output from the **flash** chip. ...

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Unified re-map and cache-index table with dual write-counters for wear-leveling of non-volatile flash RAM mass storage

RH Bruce, RH Bruce, ET Cohen... - US Patent 6,000,006, 1998 - Google Patents
 ... 7,1999 [54] UNIFIED RE-MAP AND CACHE-INDEX TABLE WITH DUAL WRITE-COUNTERS FOR WEAR-LEVELING OF NON-VOLATILE **FLASH** RAM MASS STORAGE [75] Inventors: Ricardo H. Bruce, Union City; Rolando H. Bruce, South San Francisco; Earl T. Cohen; Allan J ...
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Standardized flash controller

A Ban - US Patent 5,799,168, 1998 - Google Patents
 ... would then execute the erase procedure for that block by 5 writing an Erase (hex 20) command anywhere **within** the **flash** block to ... Identify command using the Intel 28F008 chip, standardized controller would report the number of chips present, their **interleaving** factor, and ...
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Method of pipelining sequential writes in a flash memory

ML Fandrich, RJ Durante... - US Patent 5,519,847, 1996 - Google Patents
 ... US005519847A [ii] Patent Number: [45] Date of Patent: 5,519,847 May 21,1996 [54] METHOD OF PIPELINING SEQUENTIAL WRITES IN A **FLASH** MEMORY [75] Inventors: Mickey L. Fandrich, Placerville; Richard J. Durante, Citrus Heights; Rodney R. Rozman, Placerville, all of ...
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Flash memory architecture implementing simultaneously programmable multiple flash memory banks that are host compatible

P Estakhri - US Patent 6,721,843, 2004 - Google Patents
 ... overhead data, thereby emulating the size of a data field typically available in commercial hard disks. FIG. 1 depicts a non-volatile memory array 65 **within** a **flash** memory device. A collection of Physical Sectors or Pages 108, ...
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USB smart switch with packet re-ordering for interleaving among multiple flash-memory endpoints aggregated as a single virtual USB endpoint

BW Chen, HY Chou... - US Patent 7,079,010, 2006 - Google Patents
 ... 4, 2006 [54] USB SMART SWITCH WITH PACKET RE-ORDERING FOR INTERLEAVING AMONG MULTIPLE **FLASH**-MEMORY ENDPOINTS AGGREGATED AS A SINGLE VIRTUAL USB ENDPOINT [75] Inventors: Ben Wei Chen, Fremont, CA (US); Horng-Yee Chou, Palo Alto ...
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Method and apparatus for storing location identification information within non-volatile memory devices

M Asnaashari - US Patent 6,327,639, 2001 - freepatentsonline.com
 ... In fact, generally, a controller semiconductor device coupled between the host (in the computer system) and the **flash** devices translates the logical block address (LBA) into a physical block address (PBA) and uses the latter to access the data file **within** **flash** memory. ...
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Hydra: A block-mapped parallel flash memory solid-state disk architecture

YJ Seong, EH Nam, JH Yoon, H Kim... - IEEE Transactions on ..., 2010 - computer.org
 ... 3.1 Bus-Level and Chip-Level **Interleaving**. The Hydra SSD uses **interleaving** over multiple **flash** memory buses to overcome the bandwidth limitation of the **flash** memory bus. In the bus-level **interleaving**, sectors **within** a superblock are distributed in a round-robin manner. ...
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[PDF] from csail.mit.edu

Energy efficient software-based self-test for wireless sensor network nodes

R Zhang, Z Zilic... - VLSI Test Symposium, 2006, ..., 2006 - ieeexplore.ieee.org
 ... 8 RAM W0 (ten blocks -5kBytes) 9 RAM R0 (ten blocks - 5kBytes) A RF Initialization B RF packets sending (4 packets) Figure 8 shows the current measurement result before and after time **interleaving** between **FLASH** erase and RAM testing **within** embedded memories in the ...
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